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Integrating Data-Driven Clock Gated Multibit Flip-Flops (DDCG-MBFF) for Power Savings Maximization

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ABSTRACT:

Two Data-driven clock two gated two (DDCG) two and two multibit flip-flops (MBFFs) are two low-power format methods two that two are typically handled separately. Combining these methods into a single grouping algorithm and layout two float enables two similarly two electricity two savings. We study MBFF multiplicity and its synergy with FF data-to-clock toggling probabilities. A probabilistic model is carried out to maximize the predicted energy financial savings through grouping FFs in growing two order of their data-to-clock toggling probabilities. We current a front-end format flow, guided with the aid of bodily plan issues for a 65-nm 32-bit MIPS and a 28-nm industrial community processor. It is proven to obtain the strength financial savings of 23% and 17%, respectively, in contrast with designs with normal FFs. About 1/2 of the financial savings was once due to integrating the DDCG into the MBFFs.

INTRODUCTION:

The data of digital structures are typically saved in flip-flops (FFs), each and every of which has its very very own interior clock driver. In an try to limit the clock power, a range of FFs can be grouped into a module referred to as a multibit FF (MBFF) that two properties two the clock two drivers two of all the underlying FFs. We denote the grouping of kFFs into an MBFF with the aid of a k-MBFF. twoKapoor two et two al. [1] reported two a 15% two bargain two of two the complete dynamic electricity in a 90-nm processor design. Electronic graph automation tools, such as Cadence Liberate, guide MBFF characterization.The benefits of MBFFs do now not come for free. By sharing accepted drivers, the clock slew fee is degraded, as a result inflicting a massive short-circuit cutting-edge and a longer clock-to-Q propagation prolong tpCQ. To cure this, the MBFF inside drivers can be bolstered at the fee of some increased power. It is therefore endorsed to observe the MBFF at the RTL format stage to keep away from the timing closure hurdles caused with the aid of the introduction of the MBFF at the backend structure stage. Due to the truth that the average data-to-clock two toggling ratio of FFs is very small, which generally tiers from 0.01 to 0.1 [2], the clockpower monetary savings continually outweigh the short-circuit electricity penalty of the data toggling.An MBFF grouping ought to be pushed by using the usage of logical, structural, and FF exercise considerations. While FFs grouping at the sketch stage have been studied thoroughly, the front-end implications of MBFF crew measurement and how it impacts clock gating (CG) has attracted little attention. This short responds to two questions. The first is what the exceptional bit multiplicity k of data-driven clock-gated (DDCG) MBFFs have to be. The 2nd is how to maximize the electricity financial savings based totally on data-to-clock toggling ratio (also termed pastime and statistics toggling probability).An MBFF usage at the RTL frequent experience synthesis graph stage can be decided in [3] for a 55-nm 230-MHz format of a laptop on a chip.

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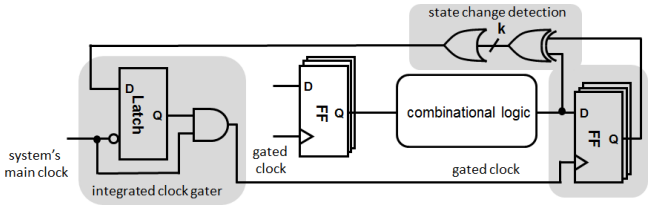

Fig. 1. DDCG integrated into a *k*-MBFF

Santos et al. [3] constrained the MBFF grouping into FFs belonging two to the same bus.

Both 2-MBFFs and 4-MBFFs had been used with a 20% make bigger in tpCQ. A dynamic strength discount of 13% was once once carried out with some degradation in timing convergence. This used to be remedied by way of capacity of applying low voltage threshold cells on quintessential paths, which pretty increased the leakage power. The entire area used to be once prolonged with the aid of 2.3%, due to the truth of the timing fixes.Most published works on MBFF have based on physical imple- mentation, pushed especially by way of the usage of the postplacement diagram [4], [5], [7], [8], [13], [16]. In these works, FF things to do tend two to be two ignored. Each FF is related with time margins derived from the diagram comprising 1-bit FFs. The wires linked to the records enter and output of an FF two are anchored on two their two opposite two facet to the two relaxation of the logic, whereas the characteristic of the FF is allowed to move round without violating timing. This defines the vicinity in the diagram the place the FF can be displaced and merged into the MBFF. The 2-MBFF merging is formulated as an optimization trouble that pastimes at maximizing the range of merged FFs. Other works [9]–[11] have added clock-tree sketch considerations as well.To in addition retailer power, [6] delivered CG, on the other hand the relationship amongst the CG strategy,

Two the FF activities, and their grouping two was once once now now not conclusive. Wang et al. [12] described each and every other postplacement algorithm that accounted two implicitly for switching information to estimate the expected power. Although [6] and [12] used switching records as a secondary criterion in postplacement FF grouping, our approach is to use it as a predominant clustering criterion, and do so at the preplacement RTL level.The requirement in [4]–[13] and [16] of having a timing-converged postplacement plan as the commencing factor for the MBFF layout waft is a burden. Timing constraints may additionally moreover be very tight, as a result limiting the manageable FF merging. Moreover, it considerably diminished.

solution house thru confining the merging to diagram proximity, whereas RTL merging is free of such constraints. No less important, having a timing-converged sketch as a prerequisite reduces the impetus to regulate the diagram to MBFFs. Our cause via distinction is that the clock-gated MBFF ought to be introduced at the RTL diagram level, primarily based definitely onarchitectural, structural, and, most importantly, FF recreation considerations.The foremost contributions of this quick are as follows:1) a plan methodology that fuses MBFF and DDCG, yielding tremendous strengthsavings;2) a probability-driven algorithm that minimizes the expected DDCG MBFF power consumption.The therest of this short is equipped as follows. Section IIdiscusses the have an impact on of data-to-clock togglingchances on strength economic savings and how it influences the integration of DDCG with MBFF.

ISSN: 1832-5505
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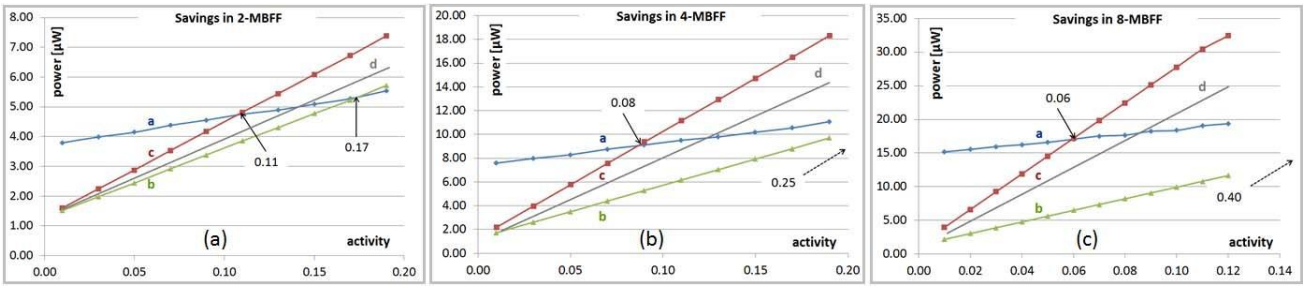


Fig. 2. Power consumption of *k* 1-bit FFs compared to k-MBFF: 2-MBFF (a), 4-MBFF (b) and 8-MBFF (c). Line (a) is the power consumed by *k* 1-bit FFs driven independently of each other. Line (b) is the ideal case of simultaneous (identical) toggling. Line (c) is the worst case of exclusive (disjoint) toggling. Line (d) is an example of realistic toggling.

Section III analyzes what FFs be grouped into the DDCG MBFF used in Section IV in a grouping algorithm and a format flow. Section V affords the experimental results, and Section VI attracts conclusions.II. INTEGRATING CLOCK GATING INTO MBFFLet p be the data-to-clock toggling probability. The anticipated energy E1 bump off by capability of a 1-bit FF isE1(p) = λ1 + µ1 p (1)where λ1 two is the electricity of the FF's indoors clock driver and µ1 is two the power of statistics toggling. In the conventional case of k-MBFF, let λk two twotwo be the strength of the MBFF's interior clock driver and µk its per-bit facts toggling energy. Assume that the FFs toggle with probabilityp independently of each other. It has been shown in [14] that the anticipated electricity isnot take into account the clock driver sharing, which also impacts the highest quality grouping as proven below.

To grasp the power savings of a *k*-MBFF achievable by DDCG, Fig. 1 two was two simulated two with SPICE two for more than a few two things to do p and okay 2, 4, 8 Fig. 2(a) shows the electricity consumption of a 2-MBFF. Line (a) is the energy ate up by means of two 1-bit FFs driven independently of every other. The 3.8-µW strength at zero exercise is due to the toggling of the clock driver at every FF, and it is constantly ateup regardless of the activity.

Line (b) corresponds to the perfect case the place the two FFs toggle simultaneously (identically). In this case, the clock driver shared via the two FFs either toggles for the sake of the two or is disabled via the interior gate shown in Fig. 1. As expected, the energy fed on for zero undertaking is smaller than two 1-bit FFs. As the undertaking increases, the electricity of line (b) rises faster than that of line (a) considering the fact that the gating circuit overhead consumes strength proportionally to the activity. There is no factor in the usage of a 2-MBFF past the 0.17 exercise crossing point, the case the place electricity begins to be lost.

It is vital to notice that toggling independence is a pessimistic assumption. In reality, the correlation between FF toggling yields higher strength financial savings than the mannequin in [2].
The ratio (kE1(p) Ek(p))/kE1(p) expresses the strength saving conceivable of k-MBFF. The coefficients λ and µ of the 65-nm 1-MBFF,
2-MBFF, and 4-MBFF were derived with SPICE simulations. Zero exercise (p 0) yields 35% financial savings for the 2-MBFF and 55% financial savings for the 4-MBFF, whereas full endeavor (p 1.0) yields 15% financial savings for the 2-MBFF and 23% financial savings for the 4-MBFF. In standard

ISSN: 1832-5505
Vol-12 Issue-01 Jan 2024

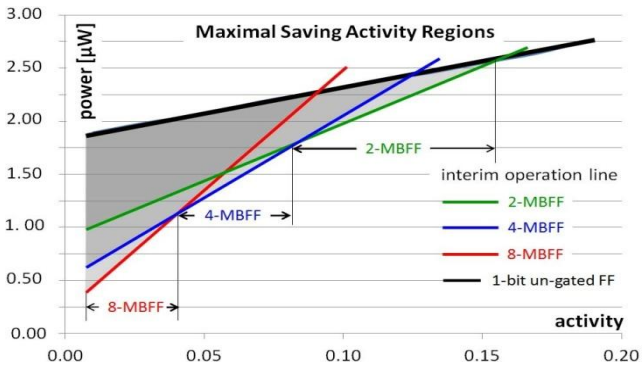
VLSI systems, the average p does not exceed 0.1, so excessive savings are achievable. Section III generalizes the electricity consumption mannequin two in (2) to the case of awesome statistics toggling probabilities. DDCG built-in into a k-MBFF. The shaded circuits reside within a library cell. Given an pastime p, the team size ok that maximizes the strength financial savings solves the equation. whereC_{FF} and C_{latch} are the clock input loads of an FF and a latch, respectively [2]. The solution to (3) for various activities is shown in Table I for typical C_{FF} and C_{latch}. The above optimizationdoesThe interim line, line (d), shown between the extreme cases oflines (b) and (c), represents a more realistic operation where FFs within an MBFF toggle neither identically nor exclusively.

Fig.2(b)showsthepowerconsumedbyth e4-MBFF,whereline(a) corresponds to four 1-bit FFs driven independently of each other, line (b) represents the best case of simultaneous toggling of the four FFs, and line (c) represents the worst case of exclusive toggling. For zero activity, the per-bit power saving is (7.4 2.2)/4 1.3μW, which is larger than the 1.0 μW in the 2-MBFF. Note, however, that for the worst case of exclusive toggling, the 4-MBFF stops saving at 0.08 activity, compared with 0.11 in the 2-MBFF. In the best case of simultaneous toggling, the 4-MBFF is always favored over the 2-MBFF. Similar conclusions hold for the 8-MBFF shown in Fig. 2(c). Its per-bit power saving for zero activity8 1.6 μW. The saving of the 8-MBFF stops at 0.06 activity in the worst case and at 0.40 in the best.

WHAT FFS SHOULD BE GROUPED IN AN MBFF?

Clearly, the best grouping of FFs that minimizes the energy consumption can be achieved for FFs whose toggling is highly correlated. Using toggling correlations for MBFF grouping has the drawback of requiring early knowledge of the value change dump.

Vectors of a typical workload. Such data may not exist in the early design stage. More commonly available information is the average toggling bulk probability of each FF in the design, which can be estimated from earlier designs or the functional knowledge of modules. FFs' toggling probabilities are usually different from each other. An important question is therefore how they affect their grouping. We show below that data-to-clock toggling probabilities matter and should be considered for energy 2-MBFFs.Wedenoteby FF(i,j) a2-MBFF,comprising FF$_i$and FF$_j$, toggling independently of each other with probabilities p_i and p_j, respectively.Whenneitheristoggling,theclock ofFF(i,j)isdisabled by the gate and the internal clock driver doesnot consume dynamicenergy. When both FF$_i$ and FF $_j$ are toggling, the clock of FF(i, j) is enabled and the clock driver energy is useful for both FFs so there is no waste. Waste occurs when one FF is toggling, but its counterpart is not, a case where the enabled clock signal drives both FFs, butonly one needs it. Waste $W(i, j)$ of half the internal clocminimization. Given$n$ FFs $\{FF_i\}^n$, let us consider their grouping in



ISSN: 1832-5505
Vol-12 Issue-01 Jan 2024

Fig. 3. Division of the activity into ranges of maximal savings.

Power savings per activity obtained by grouping an FF in the 2-MBFF, 4-MBFF, and 8-MBFF, respectively. It shows that for a very low activity, it pays to group FFs into an 8-MBFF.AsactivityMBFF overtakes and pays off more than the 4-MBFF, up to an activity where the power savings stops. The remaining FFs can be grouped into ungated MBFFs, simply to reduce the number of internal clock drivers. We take advantage of this behavior and the optimal groupingbythemonotonicactivityorderingshowninSectionIII.
The following MBFF grouping algorithm is proposed.

1) Sort the n FFs such that $p1 \leq p2 \leq \cdots \leq pn$.
2) A few practical comments are in order. The grouping should not.

CAPTURING EVERYTHING IN A DESIGNFLOW

In the following paragraphs, we combine the activity p and the MBFF multiplicity k in a design flow aimed at minimizing the expected wasted energy. Fig. 2(a)–(c) illustrates that the power savings of the 2-MBFF, 4-MBFF, and 8-MBFF, respectively, are used. Knowing the activity p of an FF, the decision as to which MBFF size k it best fits follows the interim lines, lines (d). To obtain the per-bit power consumption, lines (d) in Fig. 2(a)–(c), representing an MBFF realistic operation, were divided by their respective multiplicity. The result is shown in Fig. 3.To maximize the power savings, Fig. 3 divides the range of FF activity into regions. The black line follows the power consumed by a 1-bit ungated FF. The triangular areas bounded by the black line and each of the green, blue, and red per-bit lines show the amount

other. FFs belonging to different pipeline registers should therefore not be mixed in an MBFF. Similar arguments hold for other system buses and registers such as those storing data, addresses, counters, statuses, and the like. Another example is the FFs of finite-state machines, whose MBFF grouping should not cross control logic borders.

At last, the previously mentioned postplacement MBFF grouping must think about the planning limitations, which are incorporated with their calculations. On the other hand, the MBFF gathering calculation doesn't require express planning limitations since it works at the RTL configuration level. So as to conquer any hindrance between the RTL gathering and the gathering driven by backend timing-conclusion contemplations, we proposed suitable DDCG configuration stream. The fundamental thought includes giving "characteristic" physical design mandates for FF gathering by utilizing an earlier situation. The primary advances are portrayed underneath. More subtleties can be found in [18]:

1)estimation of the FFs flipping probabilities;
2)running the situation to get starter favored areas of FFs

EXPERIMENTALRESULTS

The proposed DDCG MBFF configuration stream was utilized for two plans: a 32-piece pipelined MIPS processor, executed in a TSMC 65-nm innovation, and a mechanical system processor, actualized in a TSMC 28-nm innovation. For the MIPS, an outstanding task at hand of sort and lattice augmentation programs was tried, as appeared in Table II. The

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Vol-12 Issue-01 Jan 2024

information to-clock flipping likelihood for each FF was inferred by mimicking the outstanding task at hand on the RTL structure.

For each test, the normal information to-clock exchanging movement of a FF in the pipelined register is appeared under the stage name. Watch the abatement in action with the advancement of the pipeline organize from guidance bring to compose back. The MBFF bits of the pipeline registers were assembled by monotonic action. Table II shows the power investment funds acquired for the consolidated benchmark. Every pipeline arrange shows the reserve funds for execution with an ungated MBFF and for DDCG incorporated into MBFFs, as proposed here. The outcomes were estimated with SpyGlass [15] recreations where the MIPS processor was worked at 1.1 V and 200 MHz. Though the ungated MBFF spared 18% of the all out power, the coordination of DDCG with MBFF yielded right around a twofold sparing of 34.6%. The pipelined registers expended 65% of the whole MIPS control (memory and IO barred), so the absolute power decrease in the whole center was 23%, including the gating overheads.To examine the advantages of front-end grouping compared with postlayout grouping, we employed ad hoc FF clustering based on their locationobtained by the Cadence Virtuoso tool. Both DDCG 2-MBFF and DDCG 4-MBFF were used depending on the FF layout proximity. The outcomes are appeared in the postlayout lines of Table II. The front-end RTL gathering outflanked the postlayout, yielding almost 41% more investment funds.

The subsequent investigation was a finished mechanical system proces-sor planned in the TSMC 28-nm innovation. The processor works in 800 MHz. It is isolated into seven units, named A–G in Table III. The first plan previously included broad clock empowering rationale signals and ungated MBFFs, embedded both by the RTL compiler and physically. Every unit contains many clock spaces inferred by rationale conditions. The DDCG MBFF configuration stream chipped away at each clock area independently. The system processor expended an aggregate of 6.2 W, of which 45% was charged to the clock organize, including its basic FFs. The first structure included ungated MBFFs, so Table III shows the net power investment funds got exclusively by the DDCG expansion appeared in Fig. 1.

The information to-clock flipping proportions of the FFs were profiled first with the guide of broad power reproductions that are as of now utilized by the enterprise for control intermingling approval. The FFs were then arranged in rising request by their information to-clock flipping likelihood and assembled by the FF action request, subject to the consistent and physical nearness limitations portrayed in Section IV.

Table III shows an extra 8% net power saving money over the ungated MBFFs in reference. The power estimations included both dynamic and static segments and all the gating overheads. The 8% control investment funds goes ahead top of the 9% reserve funds accomplished utilizing MBFFs in the first structure, subsequently yielding 17% joined reserve funds. Like the MIPS, this is about twofold the power reserve funds contrasted and ungated MBFFs alone. Such reserve funds are exceptionally valued by the business. The territory punishment because of the presentation of CG hardware was 2.3%.

CONCLUSION

This brief suggests combining MBFFs and probability-driven CG to increase their power savings. A model utilizing the relation- ship between the optimal MBFF multiplicities to FF data-to-clock toggling probabilities is used in a practical design

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Vol-12 Issue-01 Jan 2024

flow, achieving 17% and 23% power savings, compared with designs with ordi- nary FFs. About half of these savings can be attributed to the integration of DDCG into MBFFs.\

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Vol-12 Issue-01 Jan 2024

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